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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Weiguang Qiu

Assignee: Analog Microelectronics, Inc.

Title: CCFL CIRCUIT WITH INDEPENDENT ADJUSTMENT OF FREQUENCY AND DUTY CYCLE

Serial No.: 10/621,746 File Date: July 16, 2003

Examiner: Thuy V. Tran Art Unit: 2821

Docket No.: AME-007

December 15, 2004

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This Appeal Brief, filed in triplicate, is in support of the Notice of Appeal dated November 22, 2004.

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Analog Microelectronics, Inc., pursuant to the Assignment recorded in the U.S. Patent and Trademark Office on February 6, 2004 on Reel 014310, Frame 0390.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-9 are pending. Claims 1-9 stand rejected.

In the present paper, rejected Clams 1-9 are appealed.

Pending Claims 1-9 are listed in Appendix A.

IV. STATUS OF AMENDMENTS

Claims 1, 2, 3, 5, and 6 were amended in this application. All amendments were accepted.

V. SUMMARY OF THE INVENTION

To summarize Applicant's invention, paragraphs [0033]-[0037], [0039], [0043]-[0048], and [0051]-[0056] of the Specification are provided below. Figures 2, 4, and 5, which are referenced in these paragraphs, are also provided herein for convenience.

> [0033] In accordance with one feature of the invention, two independent control variables, i.e. the frequency and the duty cycle of the driving waveform to an output driver, can be used to optimize cold cathode fluorescent lamp (CCFL) operation. Specifically, the frequency of the driving waveform can be used to control the gain of a piezoelectric transformer (PZT) in the CCFL circuit. In contrast, the duty cycle of the driving waveform can be used to control the amplitude of the sinusoidal waveform at the PZT input terminal, and thus the current through the CCFL.
>
> [0034] Adjusting the frequency and the duty cycle simultaneously can result in the CCFL circuit being unstable. Therefore, in accordance with one feature of the invention, these control variables can be adjusted separately. This independent adjustment is possible based on the configuration of the CCFL circuit, wherein the frequency is a function of battery (i.e. input) voltage and the duty cycle is a function of the CCFL current.
>
> [0035] Figure 2 illustrates a simplified CCFL system 200 that includes a CCFL circuit 270. CCFL circuit 270 includes the components described in detail in reference to CCFL circuits 100A and 100B (Figures 1A and 1D, respectively). CCFL circuit 270 further includes a diode 234 connected between the output terminal of CCFL 110 and resistor 113 as well as a diode 235 connected between the output terminal of CCFL 110 and VSS. In one embodiment, battery 101 can provide a voltage source between 7-24 V (typical for 3

lithium ion cells provided in a notebook computer application).

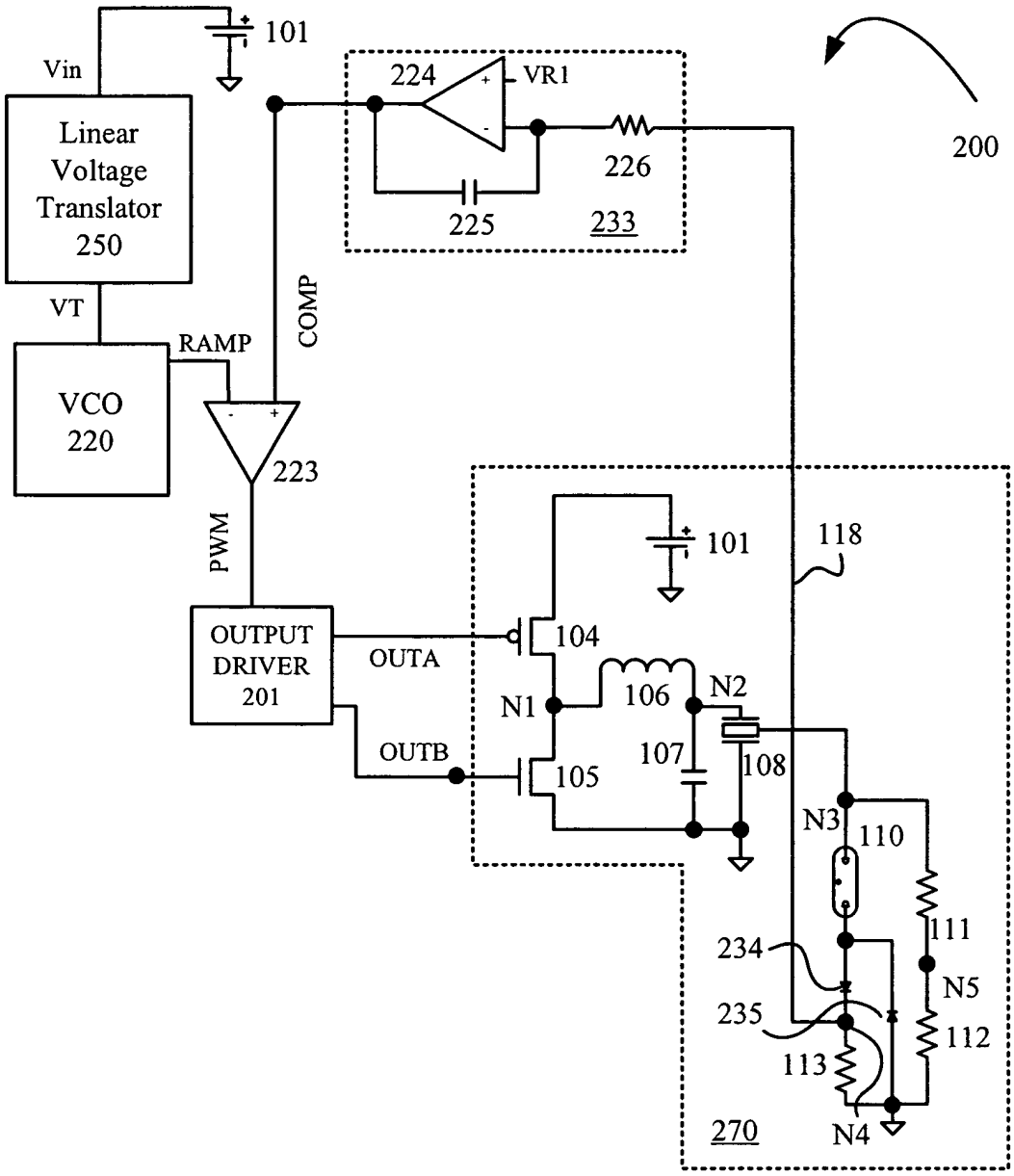


Figure 2

[0036] CCFL system 200 includes a first control loop connected to a node N4 that provides a DC signal COMP to a positive terminal of a comparator 223. System 200 further includes a VCO 220 that provides a signal RAMP (sawtooth

waveform) to a negative terminal of comparator 223. The output signal of comparator 223, i.e. a PWM signal (a square waveform), is provided to an output driver 201, which in turn provides the non-overlapping clock signals OUTA and OUTB to transistors 104 and 105 (i.e. the driving waveforms to CCFL circuit 270).

[0037] … the current through CCFL 110 can be sensed on line 118, wherein the rectified voltage across resistor 113 (ensured by diodes 234 and 235) is proportional to the CCFL current. In accordance with one feature of the present invention, that voltage can drive an input of an integrator 233.…

[0039] … The purpose of integrator 233 is to generate a DC signal COMP such that the time-averaged voltage at node N4 is substantially equal to reference voltage VR1.

[0043] In accordance with one feature of the invention shown in Figure 2, a linear voltage translator 250 can be used to provide an appropriately translated voltage VT to VCO 220. Specifically, within a known range of input voltages Vin to CCFL system 200, VCO 220 would preferably receive a predetermined range of voltages VT.

[0044] Of importance, the translated (also called control) voltage VT can be based on the PZT actually used in CCFL system 200. Specifically, the actual frequency/gain relationship … can vary from one PZT to another. Therefore, the translated voltage VT can correspond to an actual voltage that when provided to VCO 220 will provide a frequency within a range of frequencies 161 and 162 for the actual PZT used in CCFL system 200. In one embodiment, input voltages Vin could include 7-24 V (i.e. the potential voltages of battery 101) and translated voltages VT could include 0-5 V. Therefore, linear voltage translator 250 can be advantageously used to provide a predetermined range of translated voltages VT to VCO 220 based on a known range of input voltages Vin to CCFL system 200.

250

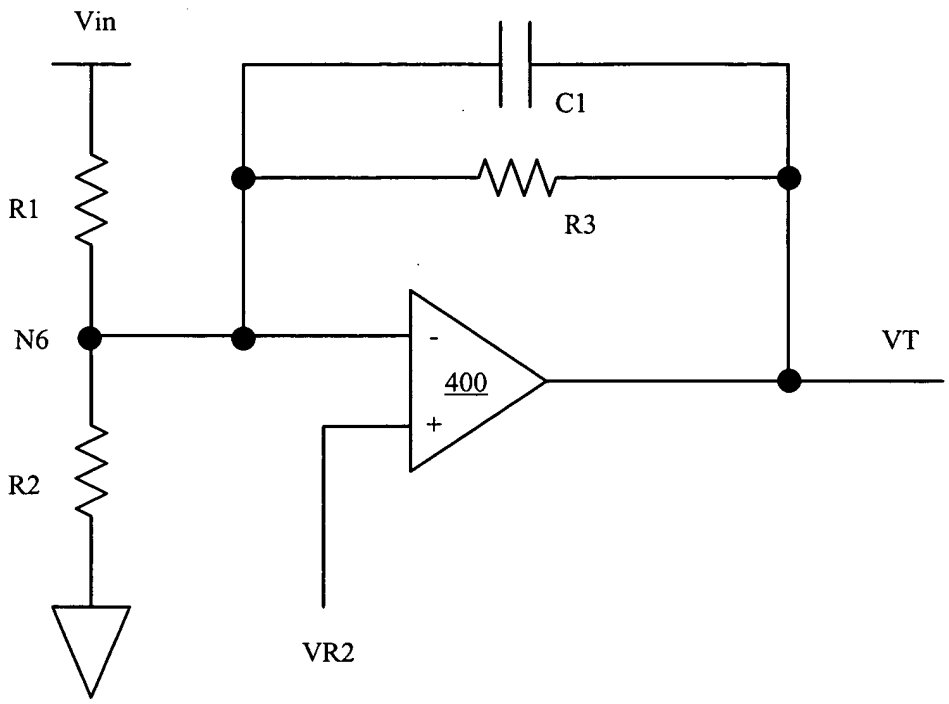


Figure 4

[0045] Figure 4 illustrates an exemplary embodiment for linear voltage translator 250. In this embodiment, two resistors R1 and R2 are connected in series between an input voltage (i.e. battery 101) and a voltage source VSS, thereby forming a voltage divider such that a node N6 (located between resistors R1 and R2) provides a voltage proportional to the voltage of battery 101. The voltage at node N6 drives the negative input terminal of an error amplifier 400. Error amplifier 400 compares the voltage at node N6 with a reference voltage VR2 received on its positive input terminal. Note that in general, reference voltage VR2 can be set in a manner similar to reference voltage VR1. A resistor R3 and a capacitor C1 are coupled in parallel between the negative input terminal and

the output terminal of error amplifier 400. Capacitor C1, an optional component of linear voltage translator 250, can provide a smoothing function, specifically to filter out high frequency components of the signal.

[0046] In accordance with one feature of the invention, the values of resistors R1, R2, and R3 can be chosen to obtain the appropriate transfer function, i.e. VT = f (Vin). The value of R1 can be chosen to be relatively large without being susceptible to parasitics. For example, in one embodiment, resistance R1 can be 100 kOhm to 1 Mohm.

[0047] The following equations can be used to compute resistances R2 and R3.

$$R2 = \frac{VR2(R1)(VT2 - VT1)}{VR2[(VT1-VT2) + (Vin2 - Vin1)] - (VT1Vin2) + (Vin1VT2)}$$

$$R3 = R1 \frac{VT1 - VT2}{Vin2 - Vin1}$$

[0048] wherein Vin1 is the lowest potential input voltage, and Vin2 is the highest potential input voltage, VT1 is the translated voltage when the input voltage Vin = Vin1, and VT2 is the translated voltage when the input voltage Vin = Vin2. Note that both resistances R2 and R3 are defined in terms of resistance R1. In one embodiment, the reference voltage VR2 can be 1.25 V, input voltage Vin1 can be 7 V, input voltage Vin2 can be 24 V, translated voltage VT1 can be 5 V, translated voltage VT2 can be 0 V, resistance R2 can be 67.6 kOhm, and resistance R3 can be 294 kOhm.

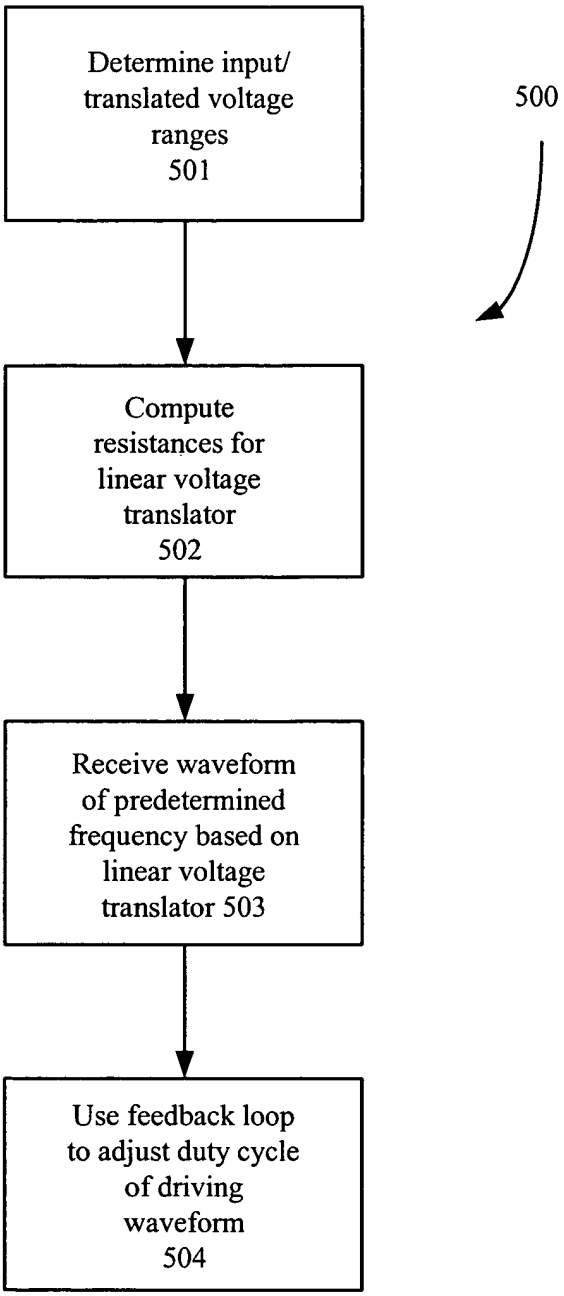


Figure 5

[0051] Figure 5 illustrates an exemplary method 500 for optimizing the operation of a CCFL circuit including a PZT. In step 501, an input voltage range for the CCFL system including the CCFL circuit can be determined. This input voltage range can include a minimum input voltage

as well as a maximum input voltage. For example, the minimum/maximum input voltages could be the potential voltage source ranges of a battery to be used in the CCFL system, e.g. 7 V and 24 V.

[0052] In step 501, a translated voltage range can also be determined. This translated voltage range can include a minimum translated voltage as well as a maximum translated voltage. In one embodiment, the minimum/maximum translated voltages VT can correspond to the actual voltages that when provided to a VCO in the CCFL system will provide the maximum/ minimum desired frequencies for the actual PZT in the CCFL system. For example, the minimum/maximum translated voltages could be 0 V and 5 V.

[0053] The voltage ranges determined in step 501 facilitate computing the resistances of a linear voltage translator in step 502. In one embodiment, the linear voltage translator includes three resistors that can advantageously translate any voltage in the potential input voltage range into a voltage in the potential output voltage range. In this manner, and described in reference to step 503, the frequency of the driving waveform can be optimized based on the PZT in the system. Note that steps 501 and 502 can be performed before operation of the CCFL system.

[0054] In step 503, which can be performed during operation of the CCFL system, the VCO in the CCFL system can receive an actual input voltage (which is within the potential input voltage range) and then generate a RAMP waveform having a predetermined frequency. Of importance, the RAMP waveform sets the frequency of the driving waveform to the predetermined frequency. The frequency of the driving waveform in turn determines the sinusoidal waveform at node N2, which controls the gain provided by the PZT. In particular, the predetermined frequency ensures that the PZT can provide an optimal gain (e.g. within +10% of the resonance frequency).

[0055] In step 504, which can also be performed during operation of the CCFL system, a feedback

loop from an output terminal of the CCFL can be used to adjust the duty cycle of the driving waveform. This duty cycle can be modified until the current through the CCFL is optimized.

[0056] Therefore, in summary, optimizing operation of the CCFL circuit includes setting an appropriate gain for the PZT using a frequency of the driving waveform and then modifying the current of the CCFL using the duty cycle of the driving waveform.

VI. ISSUES

The following issues are presented to the Board of Appeals for decision:

(A) Whether Claims 1-9 are patentable under 35 U.S.C. 102(e) over U.S. Patent Publication 2003/0160574 (Gray).

VII. GROUPING OF THE CLAIMS

Claims 1-9 stand or fall together.

VIII. ARGUMENTS

A. Claims 1-9 are patentable under 35 U.S.C. 102(e) over U.S. Patent Publication 2003/0160574 (Gray)

1. Gray: Overview

For convenience, paragraphs [0016]-[0020] and Figure 2a of Gray are provided herein.

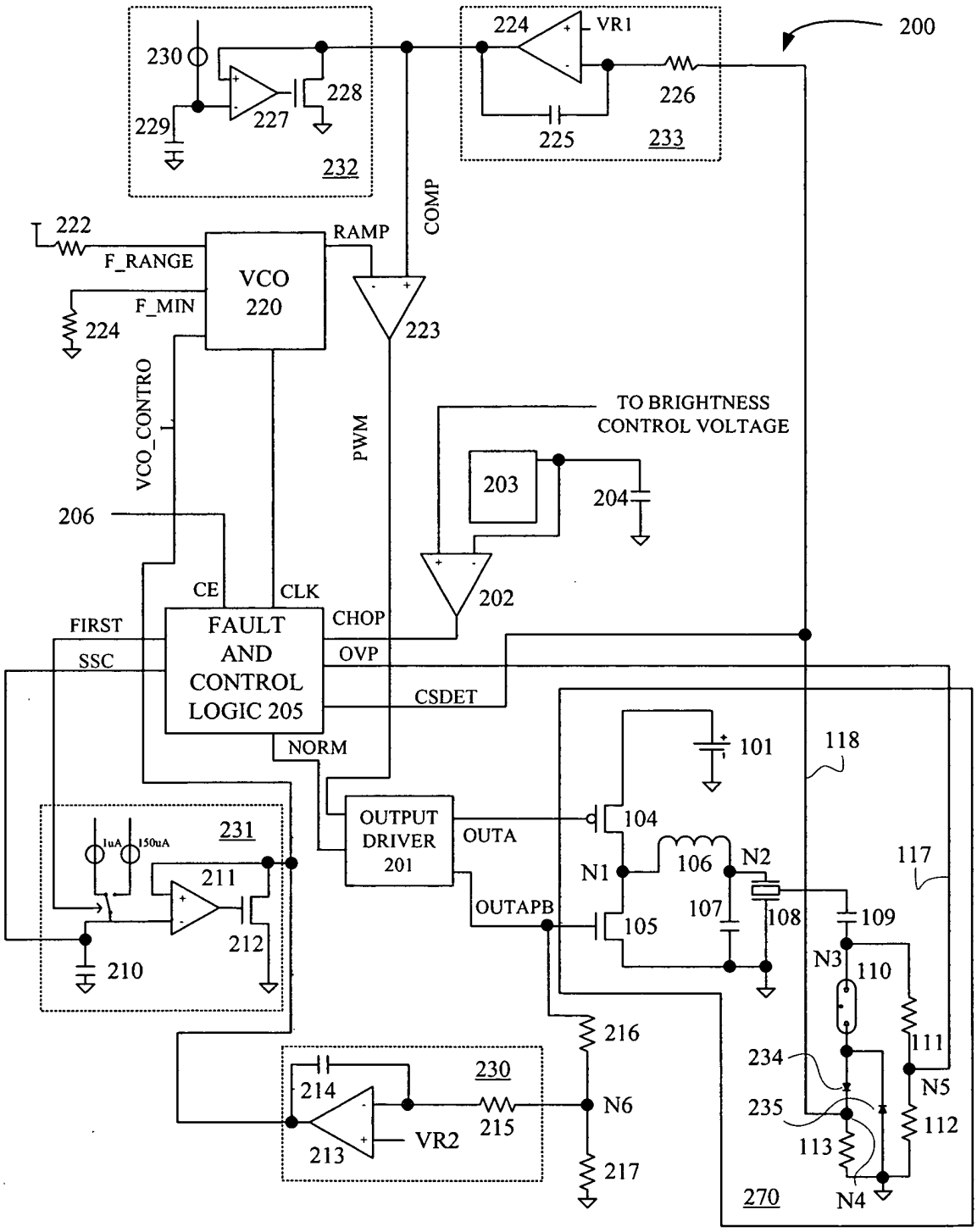
[0016] ... a frequency provided to power a cold cathode fluorescent light (CCFL) circuit is based on a duty cycle of a driving waveform to the CCFL circuit, wherein the duty cycle of the driving waveform is approximately 50%. The present invention includes a plurality of control loops to provide the above-described functionality and

other desirable functionalities. In a first control loop, a voltage of the driving waveform can be sensed by a plurality of resistors forming a voltage divider at a first node. The values of the resistors can be determined by a defined duty factor and a high level of the driving waveform. In a preferred embodiment, the defined duty factor is less than 50%.

[0017] The first loop can generate a first DC signal that is proportional to a time-averaged voltage at the first node. This function can be provided by a first integrator, which receives the voltage at the first node and a first reference voltage set in accordance with the resistor values, the defined duty factor, and the high level of the driving waveform.

[0019] In a second control loop, a voltage that is proportional to a CCFL current is sensed at a second node. A second DC signal can then be generated that is proportional to a time-averaged voltage at the second node. In one embodiment, the second DC signal can be clamped based on a current source. Specifically, the second clamp is configured to allow the second DC signal to increase at a rate that is no faster than the current source can charge a second capacitor in the clamp. In this manner, the present invention advantageously ensures a soft start-up of the CCFL circuit.

[0020] Of importance, a comparator receives both the frequency signal and the second DC signal and outputs a pulse width modulated (PWM) signal. The PWM signal generates the driving waveform for the CCFL circuit. In this manner, the PWM signal is adjusted based on the duty cycle of the driving waveform, wherein the duty cycle is approximately 50%.


200
230
228
229
227
232
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VR1
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225
233
COMP
222
F_RANGE
VCO
220
RAMP
F_MIN
224
223
VCO_CONTRO
PWM
TO BRIGHTNESS
CONTROL VOLTAGE
203
204
206
202
CE
CLK
FIRST
SSC
FAULT
AND
CONTROL
LOGIC 205
CHOP
OVP
CSDET
NORM
101
118
OUTPUT
DRIVER
201
OUTA
OUTAPB
104
105
N1
106
N2
107
108
109
117
231
1uA
150uA
211
212
210
N3
110
111
234
N5
235
112
113
N4
270
216
214
230
215
N6
VR2
213
217

Figure 2A

In reference to Figure 2A and further referring to paragraphs [0046, 0049] of Gray, the first control loop can include a node N6 and an integrator 230 that provides a signal RAMP (sawtooth waveform) to a negative terminal of comparator 223. The second control loop can include node N4, line 118, and an integrator 233 that provides a signal COMP to a positive terminal of a comparator 223. The output signal of comparator 223, i.e. a PWM signal (a pulsed waveform), is provided to an output driver 201, which in turn provides the non-overlapping clock signals OUTA and OUTAB to transistors 104 and 105 (i.e. the driving waveforms to CCFL circuit 270). Of importance, the second control loop of the present invention can be used to change the frequency of the driving waveform to transistors 104 and 105 such that its duty cycle approaches a set value (e.g. 50%), thereby increasing the efficiency of system 200. As the voltage of battery 101 increases, the oscillator frequency eventually reaches a lower limit set by the system designer. At that point, the duty cycle will decrease below its set value (e.g. 50%) to maintain proper regulation of the CCFL current.

As taught by Gray in [0057], the minimum operating frequency of VCO 220 can be set by a resistor 224, which is coupled to supply voltage VSS, whereas the adjustment range of VCO 220 can be set by a resistor 222, which is coupled to a supply voltage VDD.

2. Applicant's limitations recited in Claims 1-9 are not taught by Gray.

Claim 1 recites, "wherein a frequency of the driving waveform is based on a linearly translated input source voltage". Applicant respectfully submits that Gray fails to teach this limitation.

The Office Action cites battery 101, paragraph [0046] lines 19-23, and paragraph [0060] lines 1-2 as teaching a linearly translated input source voltage. Applicant traverses this characterization. Specifically, battery 101 can be an input source voltage, but is not a linearly translated input source voltage. Paragraph [0046] lines 19-23 of Gray states:

> As the voltage of battery 101 increases, the oscillator frequency eventually reaches a lower limit set by the system designer. At that point, the duty cycle will decrease below its set value (e.g. 50%) to maintain proper regulation of the CCFL current.

This citation does not teach a linearly translated input source voltage.

Paragraph [0060] lines 1-9 of Gray states:

> As the voltage of battery 101 increases, the frequency of the driving waveform will increase, thereby keeping the current through CCFL 110 constant until VCO 220 reaches its maximum frequency. At this point, irrespective of further increases in the battery voltage, the frequency cannot change as VCO 220 has achieved its maximum frequency. Thus, as the voltage of battery 101 increases beyond this point, the duty cycle will be decreased to maintain regulation.

This citation also does not teach a linearly translated input source voltage.

Because Gray fails to disclose or suggest "wherein a frequency of the driving waveform is based on a linearly translated input source voltage", Applicant requests reconsideration and withdrawal of the rejection of Claim 1.

Claims 2-4 depend from Claim 1 and therefore are patentable for at least the reasons presented for Claim 1. Based on those reasons, Applicant also requests reconsideration and withdrawal of the rejection of Claims 2-4.

Moreover, Claim 2 recites, "wherein the linearly translated input source voltage is based on characteristics of the PZT in the CCFL circuit". The Office Action generically cites Figure 2A of Gray as teaching this limitation. Applicant submits that Figure 2A does not disclose or suggest this limitation and therefore requests further reconsideration and withdrawal of the rejection of Claim 2.

Moreover, Claim 3 recites, "wherein the linearly translated input source voltage is based on a potential input voltage range for the CCFL circuit". The Office Action cites battery 101 and paragraph [0050] lines 5-6 for CCFL circuit 270 as teaching this limitation. The battery 101 fails to teach a linearly translated source voltage, much less a linearly translated source voltage based on a potential input voltage range for the CCFL circuit. Paragraph [0050] lines 5-6 indicates that the reference voltage VR1 can be between 0.5 V and 3.0 V. Gray teaches that integrator 233, which uses reference voltage VR1, controls the duty cycle of the driving waveform, not the frequency of the driving waveform. Therefore, Applicant requests further reconsideration and withdrawal of the rejection of Claim 3.

Claim 5, recites, "before operation of the CCFL circuit, determining a frequency of a driving waveform for the CCFL circuit, wherein the frequency is based on a range of input source voltages and a range of desired linearly translated source voltages associated with the PZT" and therefore is patentable for substantially the reasons presented for Claims 1 and 2. Based on those reasons, Applicant also requests reconsideration and withdrawal of the rejection of Claim 5.

Claim 6, as amended, recites, "means for determining a frequency of a driving waveform for the CCFL circuit, wherein the frequency is based on a range of input source voltages and a

range of desired linearly translated source voltages associated with the PZT" and therefore is patentable for substantially the reasons presented for Claims 1 and 2. Based on those reasons, Applicant also requests reconsideration and withdrawal of the rejection of Claim 6.

Claim 7 depends from Claim 6 and therefore is patentable for at least the reasons presented for Claim 6. Based on those reasons, Applicant also requests reconsideration and withdrawal of the rejection of Claim 7.

Moreover, Claim 7 recites:

> a first resistor coupled between a node and a high voltage source, wherein the high voltage source is one voltage in the range of input source voltages;
> a second resistor coupled between the node and a low voltage source;
> an error amplifier having a positive input terminal connected to a reference voltage and a negative input terminal; and
> a resistor transistor coupled to the node, the negative input terminal of the error amplifier, and an output terminal of the error amplifier.

The Office Action cites resistors 215, 216, 217 and error amplifier 213 (see Figure 2A above) as teaching these limitations. Applicant traverses this characterization. For example, transistor 216 is not coupled to a high voltage source. Specifically, line/signal OUTAPB cannot be characterized as a one voltage in the range of input source voltages. Additionally, integrator 230 must include a capacitor 214 to generate the time-averaged voltage at node N6. Therefore, resistor 215 cannot be characterized as being coupled to an output terminal of the error amplifier. Based on these reasons, Applicant requests further reconsideration and withdrawal of the rejection of Claim 7.

Claim 8 recites:

> a first resistor coupled between a node and a high voltage source, wherein the high voltage source is one voltage in the range of input source voltages;
> a second resistor coupled between the node and a low voltage source;
> an error amplifier having a positive input terminal connected to a reference voltage and a negative input terminal; and
> a third resistor coupled to the node, the negative input terminal of the error amplifier, and an output terminal of the error amplifier.

Therefore, Claim 8 is patentable for substantially the reasons presented for Claim 7. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 8.

Claim 9 depends from Claim 8 and therefore is patentable for at least the reasons presented for Claim 8. Based on those reasons, Applicant also requests reconsideration and withdrawal of the rejection of Claim 9.

IX. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 1-9 are erroneous, and reversal of these rejections is respectfully requested.

Respectfully submitted,

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12/15/2004 Rebecca A. Baumann
Date Signature: Rebecca A. Baumann

X. APPENDIX A

1. (Previously Amended) A method of optimizing performance of a cold cathode fluorescent lamp (CCFL) circuit, the CCFL circuit including a CCFL and a piezoelectric transformer (PZT) for driving the CCFL, the method comprising:

providing a driving waveform to the CCFL circuit,

wherein a frequency of the driving waveform is based on a linearly translated input source voltage, and

wherein a duty cycle of the driving waveform is based on a detected current through the CCFL.

2. (Previously Amended) The method of Claim 1, wherein the linearly translated input source voltage is based on characteristics of the PZT in the CCFL circuit.

3. (Previously Amended) The method of Claim 2, wherein the linearly translated input source voltage is based on a potential input voltage range for the CCFL circuit.

4. (Original) The method of Claim 1, wherein providing the driving waveform includes turning on/off transistors of a half bridge in the CCFL circuit.

5. (Previously Amended) A method of optimizing performance of a cold cathode fluorescent lamp (CCFL) circuit, the CCFL circuit including a CCFL and a piezoelectric transformer (PZT) for driving the CCFL, the method comprising:

before operation of the CCFL circuit, determining a frequency of a driving waveform for the CCFL circuit, wherein the frequency is based on a range of input source voltages and a

range of desired linearly translated source voltages associated with the PZT; and

during operation of the CCFL circuit, adjusting a duty cycle of the driving waveform based on a detected current through the CCFL.

6. (Previously Amended) A system for optimizing performance of a cold cathode fluorescent lamp (CCFL) circuit, the CCFL circuit including a CCFL and a piezoelectric transformer (PZT) for driving the CCFL, the system comprising:

means for determining a frequency of a driving waveform for the CCFL circuit, wherein the frequency is based on a range of input source voltages and a range of desired linearly translated source voltages associated with the PZT; and

means for adjusting a duty cycle of the driving waveform based on a detected current through the CCFL.

7. (Original) The system of Claim 6, wherein the means for determining the frequency of the driving waveform includes:

a first resistor coupled between a node and a high voltage source, wherein the high voltage source is one voltage in the range of input source voltages;

a second resistor coupled between the node and a low voltage source;

an error amplifier having a positive input terminal connected to a reference voltage and a negative input terminal; and

a resistor transistor coupled to the node, the negative input terminal of the error amplifier, and an output terminal of the error amplifier.

8. (Original) A linear voltage translator comprising:

a first resistor coupled between a node and a high voltage source, wherein the high voltage source is one voltage in the range of input source voltages;

a second resistor coupled between the node and a low voltage source;

an error amplifier having a positive input terminal connected to a reference voltage and a negative input terminal; and

a third resistor coupled to the node, the negative input terminal of the error amplifier, and an output terminal of the error amplifier.

9. (Original) The linear voltage translator of Claim 8, wherein the output terminal of the error amplifier provides a signal to a voltage controlled oscillator (VCO) to determine an output frequency of the VCO.

IFW

PTO/SB/21 (05-03)
Approved for use through 04/30/2003. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/621,746
Filing Date	07/16/2003
First Named Inventor	Weiguang Qiu
Art Unit	2821
Examiner Name	Thuy V. Tran
Total Number of Pages in This Submission: 24	**Attorney Docket Number** AME-007

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Terminal Disclaimer
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Statement Under 37 CFR 3.73(b)
- ☐ Change In Entity Status
- ☐ Request for Refund
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Additional Enclosure(s) *(please identify below):*
  - Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY OR AGENT

Firm *or* Individual name	Jeanette S. Harms, Reg. No. 35,537, BEVER, HOFFMAN & HARMS, LLP (Customer No. 022888).
Signature	
Date	December 15, 2004

CERTIFICATE OF MAILING

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Signature	Rebecca A. Baumann	Date	December 15, 2004

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMV 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

FEE TRANSMITTAL For FY 2005

☒ Applicant claims small entity status. See 37 C.F.R. § 1.27

TOTAL AMOUNT OF PAYMENT ($) 250.00

Complete if Known	
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Filing Date	07/16/2003
First Named Inventor	Weiguang Qiu
Examiner Name	Thuy V. Tran
Art Unit	2821
Attorney Docket No	AME-007

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☒ Deposit Account Deposit Account Number: **50-0574** Deposit Account Name: **Bever, Hoffman & Harms, LLP**

For the above-identified deposit account, the Director is hereby authorized to; (check all that apply)

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☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	**Fees Paid ($)**
Utility	300	150	500	250	200	100	$
Design	200	100	100	50	130	65	$
Plant	200	100	300	150	160	80	$
Reissue	300	150	500	250	600	300	$
Provisional	200	100	0	0	0	100	$

2. EXCESS CLAIM FEES

Fee Description	Fee($)	Small Entity Fee($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee($)	**Fee Paid ($)**	Multiple Dependent Claims	
	- 20 or HP =	x	=	Fee($)	Fee($)

HP = highest number of total claims paid for, if great than 20

Indep. Claims	Extra Claims	Fee($)	**Fee Paid ($)**
	- 3 or HP =	x	=

HP = highest number of total claims paid for, if great than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 USC 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee($)	Fee Paid ($)
- 100 =	5- = (round up to a whole number)	x		=

4. OTHER FEE(S)

	Fee Paid ($)
Non-English Specification - $130 fee (no small entity discount)	
Other: Appeal Brief	$250.00

SUBMITTED BY

Signature:	Registration No. 35,537	Telephone: (408) 451-5907
Name (Print/Type) Jeanette S. Harms		Date: December 15, 2004

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on December 15, 2004.

Date: 12/15/2004 Signature: Rebecca A. Baumann

Rebecca A. Baumann